Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

1. (Currently amended) A method comprising:

executing software instructions using a processor to develop ~~developing~~ a more detailed description of a phase lock loop system by substituting, into a monomial or posynomial equation that is part of a family of monomial and posynomial expressions that describe functional characteristics of said PLL at the system level, a lower level expression that describes a characteristic of one said PLL's basic building blocks;

constructing a geometric problem with the lower level expression; and

solving the geometric problem to generate the more detailed description of the phase lock loop system, the more detailed description of the phase lock loop system comprising a transistor-level netlist.

2. (Currently amended) The method of claim 1, further comprising:

recognizing a variable within the monomial or posynomial expression for one of the functional characteristics of said PLL as having a dependency on the lower level expression~~; and~~

~~constructing a geometric problem with the lower level expression~~.

3. (Original) The method of claim 2, further comprising substituting the lower level expression into the monomial or posynomial equation to replace the variable within the monomial or posynomial expression.

4. (Canceled).

5. (Currently amended) A machine-readable medium embodying instructions, the instructions, when executed by a processor, causing the processor to perform operations comprising:

developing a more detailed description of a phase lock loop system by substituting, into a monomial or posynomial equation that is part of a family of monomial and posynomial expressions that describe functional characteristics of said PLL at the system level, a lower level expression that describes a characteristic of one said PLL's basic building blocks;

constructing a geometric problem with the lower level expression; and

solving the geometric problem to generate the more detailed description of the phase lock loop system, the more detailed description of the phase lock loop system comprising a transistor-level netlist.

6. (Currently amended) The machine-readable medium in claim 5, wherein the operations further comprise:

recognizing a variable within the monomial or posynomial expression for one of the functional characteristics of said PLL as having a dependency on the lower level expression~~; and~~

~~constructing a geometric problem with the lower level expression~~

7. (Original) The machine-readable medium in claim 6, wherein the operations further comprise substituting the lower level expression into the monomial or posynomial equation to replace the variable within the monomial or posynomial expression.

8. (Canceled).